REMARKS

Claims 1, 3, and 10-20 will be pending after entry of this amendment. Claim 1 has been amended for stylistic and typographical reasons. Claims 12 and 16 have been amended for reasons of clarity and lack of antecedent basis, respectively. Support for the amended claims can be found in the specification. No new matter has been added.

Claims 12 and 16 have been rejected under 35 U.S.C. § 112. Claims 1, 3, and 10-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Deering et al., United States patent number 5,745,125. Reconsideration of the rejections and allowance of the rejected claims in light of the amendments and remarks is respectfully requested.

Formalities

The rejections of claims 12 and 16 under 35 U.S.C. § 112 have been obviated by amendment.

Claim 1

Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Deering et al. But Deering et al. do not show or suggest each and every element of this claim.

The structures disclosed by Deering et al. and the specification of this application are superficially similar in that they have several types of blocks in common. But the structure recited in the claim is not the same as that of the cited reference. For example, claim 1, as amended, recites "a first shared operand unit coupled to the first MAC unit and the second MAC unit for providing a first shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands." Deering et al. do not show or suggest this limitation.

The office action cites the SRAM 153 of Deering et al. as corresponding to the shared operand unit recited by the claim. (Office action of October 22, 2001, page 3, first paragraph.) Assuming *arguendo* that an SRAM does correspond to a shared operand unit, a review of the figures shows that the SRAM 153 of Deering et al. is not "coupled to the first MAC unit and the second MAC unit" as required.

An examination of the schematics in Deering et al. shows this. At a high level, Figure 3 of Deering et al. show SRAM 153 coupled to a "Float" 152. Figure 6 shows the SRAM 153 coupled to an F-Core 352 in the "Float" 152. At a more detailed level, Figure 11 shows the SRAM is coupled to only one multiplier/accumulator structure, specifically that formed by FMUL 514 and FADD 516. Thus, the SRAM 153 is not coupled to a second MAC unit as required by the claim.

Among other features, the shared operand unit provides operands to multiple MAC units, thus helping the array processor efficiently perform calculations. The cited prior art does not provide this feature. Rather, applicant submits that operands are not shared, but need to be stored in two SRAMs 153 to be processed by two multiplier/accumulator structures 514, 516. Thus, the cited prior art does not provide the benefits of this claim.

For at least this reason, claim 1 should be allowable.

Claim 10

Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Deering et al. But Deering et al. do not show or suggest each and every element of this claim. For example, claim 10 recites "a plurality of shared operand circuits coupled to said plurality of multiplier/accumulator circuits for providing a shared operand to at least two of said plurality of multiplier/accumulator circuits."

As above, the cited prior art discloses a structure where each SRAM 153 provides a shared operand to only one multiplier/accumulator 514, 516. Accordingly, Deering et al. do not show or suggest "providing a shared operand to at least two of said plurality of multiplier/accumulator circuits" as required by the claim

For at least this reason, claim 10 should be allowable.

Other Claims

Claim 3 depends from claim 1, and should be allowable for at least the same reason as claim 1, and for the additional limitations it recites.

Claims 11-20 depends from claim 10, and should be allowable for at least the same reason as claim 10, and for the additional limitations they recite.

Clarification Regarding Error in Preliminary Amendment

A preliminary amendment was filed in this case on April 19, 2001. Upon review, a discrepancy between claim 1 as submitted and claim 1 in the Version With Markings to Show Changes Made was found. Specifically, the portion of claim 1 as submitted on page 2, line 8, read:

to the interface circuit to receive information therefrom and connected to the embedded.

The portion of claim 1 in the Version With Markings to Show Changes Made on page 6, line 9, read:

to the interface circuit to receive information therefrom and directly connected to the embedded. (underlining in original.)

The word "directly" was inadvertently included in the Version With Markings to Show Changes Made, and was not in claim 1 as submitted. Applicant understands that claim 1 as submitted is controlling, so the word "directly" is not now part of the claim, and does not now need to be removed by edit.

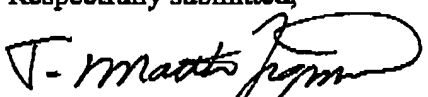
The undersigned regrets any confusion this may have caused.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this application are in condition for allowance. The issuance of a formal notice of allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-752-2456.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) An integrated circuit for image frame rendering and DSP applications, the integrated circuit during operation operating with memory, the integrated circuit comprising:

an interface circuit configured to control access to said memory, the interface circuit coupled to said memory;

an embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom; and

an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom and connected to the embedded processor via an internal bus; **[and]**

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a first shared operand unit coupled to the first MAC unit and the second MAC unit for providing a first shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other; and

wherein the array processor further comprises:

a second shared operand unit coupled to a third MAC unit and a **[forth]** fourth MAC unit for providing a second shared operand to the third MAC unit and the **[forth]** fourth MAC unit.

12. (Amended) The integrated circuit according to claim 10 wherein **[separate instruction and data streams are maintained for said array processor]** a first instruction stream and a first data stream is maintained for said array processor, and a second instruction stream and a second data stream is maintained for said embedded processor.

16. (Amended) The integrated circuit according to claim 10 further comprising:

a global external bus unit for providing an interface **[between]** to said integrated circuit **[and said external environment]**, said global external bus unit coupled to said embedded microprocessor by a system bus and by a separate dedicated bus.